REMARKS

In response to the above-identified Office Action, the Applicant submits the below remarks and respectfully requests reconsideration of the application, as amended, in light of these remarks.

The Examiner rejected claims 1-3 under 35 U.S.C. 102 (b) as being anticipated by U.S. Patent 5,434,093 (hereinafter Chau). The Examiner also rejected claims 7-9 under 35 U.S.C. 102 (b) as being anticipated by U.S. Patent 5,448,094 (hereinafter Hsu). Furthermore, the Examiner rejected claims 4-6 under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent 5,567,966 (hereinafter Hwang) in view of Chau. The Applicant respectfully traverses this rejection for the reasons set out below.

The Applicant contends that none of the cited references, alone or in combination, does not teach or suggest all limitations of claim 1, or the other independent claims of the present application. The Applicants' arguments shall be presented with respect to claim 1. However, these comments are applicable to the other independent claims of the present application, and the Examiner is respectfully requested to consider these comments and remarks when reviewing the other independent claims for allowability.

With respect to claim 1, Chau does not disclose a portion of the dialectic layer overlaying an inner-most portion of the extension. As illustrated in Figure 3e of Chau, the dielectric layer 312 does not overlay the tip regions 315a and 315b, but rather is just adjacent to the source/drain extensions. Nowhere in the reference, there is a teaching or suggestion that the dielectric layer overlies the tip regions 315a and 315b.

Moreover, with respect to claim 4, the Office Action acknowledges that Hwang does not disclose the extension extending to a more shallow depth within the substrate than the source/drain terminals to which it corresponds. However, Hwang also does not disclose the source/drain terminals comprising an extension. In Hwang source/drain regions are indicated by a reference numeral 24 in Figure 6 and LDD regions are

indicated by reference numeral 22 in Figure 6. LDD regions are not extensions of the source/drain regions in Hwang.

Furthermore, with respect to claim 7, Hsu does not disclose the source/drain terminals comprising an extension. Hsu discloses N+ doped source/drain areas 30. Hsu also discloses N- doped source/drain areas 31 which are separate areas than source/drain areas 30, and nowhere in the Hsu reference there is a disclosure or suggestion that source/drain areas 30 comprise source/drain areas 31. On the contrary, all the Figures of Hsu illustrates two separate areas 30 and 31 that are formed by separate processes as described in Column 3, lines 52-67.

The Applicant submits that the rejections under 35 U.S.C. § 102 (b) and 103 (a) have been addressed, and withdrawal of these rejections is respectfully requested. The Applicant furthermore submits that all pending claims are in condition for allowance, which is earnestly solicited.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Saina S. Shamilov
Reg. No. 48,266

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720 – 8300

MARKED UP VERSION OF THE CLAIMS

Please amend the following claims.

1. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

2. (Amended)The transistor of Claim 1, further comprising a portion of the gate electrode that overlies [an] the innermost portion of the source/drain extension [:].

3. (Amended) The [structure] transistor of Claim 2, wherein the gate electrode conforms to the recessed channel.

4. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

5. (Amended) The transistor of Claim 4, wherein a portion of the gate electrode [that] overlies an innermost portion of the source/drain extension.

7. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

8. (Amended) The transistor of Claim [6] 7, wherein a portion of the gate electrode [that] overlies an innermost portion of the source/drain extension.

9. (Amended) The transistor of Claim [6] 7, wherein the gate electrode conforms to the recessed channel.